

## WHAT IS CLAIMED IS:

1. An electromechanical system for testing IC-chips; said system being comprised of:

a total of N chip holding subassemblies, where N is an integer greater than one and where each chip  
5 holding subassembly has sockets for holding a group of IC-modules that include said IC-chips;

a moving means for automatically moving the i-th one of said N chip holding subassemblies from a load position in said system to a test position in said  
10 system, and visa-versa, where i changes with time in a sequence;

a power supply means which sends electrical power only to those IC-modules that are held by said chip holding subassemblies at said test position; and,

15 a signal generator means which sends test signals concurrently to said IC-chips on all chip holding subassemblies that are at said test position, where said test signals are shifted in time from one subassembly to another.

2. A system according to claim 1 where in said signal generator means begins to send said test signals to said IC-chips that are on the i-th chip holding subassembly, between the time that subassembly is moved  
5 to said test position and the time that the next chip holding subassembly in said sequence is moved to said test position.

3. A system according to claim 2 wherein said sequence in which said moving means moves said i-th chip holding subassembly in a repetitive sequence.

4. A system according to claim 2 wherein said sequence in which said moving means moves said i-th chip holding subassembly in a random sequence.

5. A system according to claim 2 wherein said moving means moves said i-th chip holding subassembly from said load position to said test position, and visa-versa, while at least half of said N chip holding  
5 subassemblies are at said test position.

6. A system according to claim 2 wherein said signal generator means includes N digital state machines, one on each of said N chip holding subassemblies, and a master controller which is stationary and is coupled via  
5 a communication channel to each of said N digital state machines.

7. A system according to claim 2 wherein said signal generator means sends test signals which place said IC-chips in a predetermined state but do not functionally test said IC-chips.

8. A system according to claim 2 wherein said signal generator means sends test signals which functionally test said IC-chips.

9. A system according to claim 2 which further includes a chip handler means, which is time-shared by all of said chip holding subassemblies, for moving said IC-modules from one source container into the sockets on  
5 said i-th chip holding subassembly at said load position, and from those sockets to at least one pass container and one fail container.

10. A system according to claim 9 which further includes a means for automatically replacing any one of said containers when chip handler means has emptied or filled that container with said IC-modules.

11. A system according to claim 9 wherein each socket on said chip holding subassembly faces downward at said load and test position, and said chip handler means flips each IC-module 180° from an initial position where  
5 said electrical terminals face downward.

12. A system according to claim 2 wherein each chip holding subassembly is manually removable from said system at said load position, and manually returnable to said system at said load position.